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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,519	11/17/2003	Simon Charles Watt	550-480	6837

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NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
ABEDIN, SHANTO	
ART UNIT	PAPER NUMBER
2136	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,519	WATT ET AL.	
	Examiner	Art Unit	
	SHANTO M Z ABEDIN	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-2, 4- 11, 13-25, 27-34 and 36-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4- 11, 13-25, 27-34 and 36-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/15/2008 has been entered.

2. Claims 1-2, 4- 11, 13-25, 27-34 and 36-47 are currently presented for the examination.

3. Claims 1-2, 4- 11, 13-25, 27-34 and 36-47 have been rejected.

Response to Arguments

4. The applicant's arguments regarding previous 35 USC 103(a) type rejections are fully considered, however, found not persuasive. In particular, the applicant primarily argues that (a) combination of the cited references Christie et al and Knight fails to disclose processor being operable to select said exception handler from among a plurality of possible exception handlers in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table for said exception condition and in dependence upon whether said processor is operating in said secure domain or said non-secure domain; and (b) programmable configurations associated therewith that control triggering of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode with any change of domain also being triggered when required; and (c) the examiner has no reason or motivation for combining the references Christie et al and Knight .

In response to the applicant's arguments (a) and (b), the examiner respectfully disagrees with the applicant since upon further examination, the combination of the cited references Christie et al and Knight was found to teach the limitations set forth by above arguments.

In particular, reference Christie et al teaches processor being operable to select said exception handler from among a plurality of possible exception handlers in dependence upon an exception vector value associated with said exception condition and in dependence upon whether said processor is operating in said secure domain or said non-secure domain (Fig 1, Fig 3; Col 4, line 29-67; Col 9, line 62- Col 10, line 67; Claims 1-9; exception/ interrupt handler based on whether processor/ system is operating in secure/ protected mode or insecure/ normal modes) ; and programmable configurations associated therewith that control triggering of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode with any change of domain also being triggered when required (Fig 3; Col 4, line 29-67; Col 9, line 62- Col 10, line 67; Claims 1-9; controller, or mode capable processor to control exception handling based on modes/ domains)

Furthermore, reference Knight teaches processor being operable to select said exception handler from among a plurality of possible exception handlers in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table for said exception condition and in dependence upon whether said processor is operating in said secure domain or said non-secure domain (Par 0007, 0015-0019; Claims 1-24; exception vector table for exception, and exceptions having corresponding operational modes such as normal, protected/ private, and IRQ modes) and programmable configurations associated therewith that control triggering of either a non-secure exception handler operating in a non-secure mode or a

secure exception handler operating in a secure mode with any change of domain also being triggered when required (Par 0007, 0015-0019; Claims 1-24; processor for exception handing where each exceptions has corresponding operational modes, and exception handling depend on mode of operations)

Therefore, the combination of references does teach the limitations set forth by the applicant's arguments (a) and (b).

In response to the applicant's argument (c) that there is no suggestion to combine the references Christie et al and Knight , the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both of the references Christie et al and Knight are analogous art because they are from the same field of endeavor of secure exception handling involving different operational/ execution modes. Therefore, at the time of invention it would have been obvious to a person of ordinary skill in the art to combine the teachings of Knight with Christie et al to design a method further including exception vector table in order to provide an alternative and efficient exception handling mechanism.

Therefore, previous 35 USC 103(a) type rejections of claims 1-2, 4- 7, 11, 13, 20-25, 27-30, 34, 36, and 43-47 in view of Christie et al and Knight are maintained.

5. Upon further examination and consideration, previous 35 USC 103(a) type rejections of claims 8-10, 14-19, 31-33 and 37-42 in view of Christie et al and Knight are withdrawn.

6. The examiner notes, upon further search, new grounds of rejection were found, and the applicant's above arguments are also moot in view of new grounds of rejections presented in this office action (please see below)

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1-2, 4- 11, 13-25, 27-34 and 36-47 of the instant application are provisionally rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 1- 67 of copending Application No. 10/714518.

Regarding claims 1 and 24, they are unpatentable over claims 1, 8, 12, 17-22, 34 and 53-56 of copending application no. 10/714518.

Regarding claims 2, 4-8 and 25, 27-31, they are unpatentable over claims 4-16 and 38-45 of copending application no. 10/714518.

Regarding claims 9-10 and 32-33, they are unpatentable over claims 1-4, 19-20, 34-38 and 52-54 of copending application no. 10/714518.

Regarding claims 11, 13-23 and 34, 36-47 they are unpatentable over claims 23-33 and 56-67 of copending application no. 10/714518.

Although the conflicting claims are not identical, they are not patentably distinct from each other because all the elements/ features of claim-set of the instant application either exist in similar or different names, or being obvious over the conflicting claim-set of the copending application no. 10/714518.

In particular, difference between the conflicting claims of the instant application and the copending application is that while the instant application claim set recites storing exception vectors in an active exception vector table, the copending application claim set only recites that exception/ interrupt handling is dependent upon an exception/ interrupt vector value. However, at the time of invention it would have been obvious to a person of ordinary skill in the art to store such interrupt/ exception vectors in a interrupt/ exception vector table in order to provide a managed, and efficient interrupt/ exception handling or monitoring.

This is a provisional obviousness –type double patenting rejection because the conflicting claims have not in fact been patented.

8. Claims 1-2, 4-9, 11, 13-14, 20-25, 27-32, 34, 36-37 and 43-47 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-11 of commonly assigned U.S. Patent No. 7,117284 B2.

Regarding claims 1-2, 4- 7, 11, 13, 20-25, 27-30, 34, 36 and 43-47 of the instant application, they are unpatentable over claims 1-2, 5-7 and 10 of the U.S. Patent No. 7,117284.

Regarding claims 1, 8-9, 14, 22-23, 24, 31, 32 and 37 of the instant application, they are unpatentable over claims 1, 3, 4, 6, 8 and 9 of the U.S. Patent No. 7,117284.

Although the conflicting claims are not identical, they are not patentably distinct from each other because all the elements/ features of claim-set of the instant application either exist in similar or different names, or being obvious over the conflicting claim-set of the U.S. Patent No. 7,117284 B2.

In particular, difference between the conflicting claims of the instant application and the copending application is that while the instant application claim set recites storing exception vectors in an active exception vector table, copending application claim set only recites a vectored interrupt controller operable to generate exception handling address . However, at the time of invention it would have been obvious to a person of ordinary skill in the art to design an apparatus/ vectored interrupt controller to store such vectored interrupts/ exceptions in a interrupt/ exception vector table in order to provide a managed, and efficient interrupt/ exception handling or controlling.

This is an obvious type double patenting rejection.

9. Claims 1-2, 4- 11, 13-25, 27-34 and 36-47 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-17 of commonly assigned U.S. Patent No. 7,305,712 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the similar reasons already stated in earlier paragraphs. Furthermore, at the time of invention, differences between the conflicting claim set would be obvious to a person of ordinary skill in art for the reasons already stated in earlier paragraphs. This is an obvious type double patenting rejection.

10. Claims 1-2, 4- 11, 13-25, 27-34 and 36-47 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-15 of commonly assigned U.S. Patent No. 7,124,274B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the reasons already stated in earlier paragraphs. Furthermore, at the time of invention, differences between the conflicting claim set would be obvious to a person of ordinary skill in art for the reasons already stated in earlier paragraphs. This is an obvious type double patenting rejection.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

11. Claim 47 is rejected under 35 USC 101 because of being directed to non-statutory subject matter.

Regarding claim 47, it is directed to computer program product, however, since specification does not disclose expressly nature of such program product, the examiner interprets such program product as a software per se product, and therefore, being non-statutory. See MPEP 2106.01

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1-2, 4- 7, 11, 13, 20-25, 27-30, 34, 36, and 43-47 are rejected under 35 USC 103 (a) as being unpatentable over Christie et al (US 7165135 B1) in view of Knight (US 2003/0126520 A1)

Regarding claims 1 and 24, Christie et al discloses apparatus/ method for processing data, said apparatus/ method comprising:

a processor operable in a plurality of modes and a plurality of domains, said plurality of domains comprising a secure domain and a non-secure domain (Fig 1; related modes and domains; Col 4, starting at line 7, plurality of memory location associated with the plurality of the execution modes) said plurality of modes including:

at least one secure mode being a mode in said secure domain (Fig 1; secure modes and domains; Col 4, starting at line 7, plurality of memory location associated with the plurality of the execution modes) ; and

at least one non-secure mode being a mode in said non-secure domain (Fig 1; related modes and domains; Col 4, starting at line 7, normal mode and domain); wherein when said processor is executing a program in a secure mode said program has access to secure data which is not accessible when said processor is operating in a non-secure mode (Fig 1; Col 4, starting at line 65; Col 9, starting at line 62; Claim 1)

said processor is responsive to one or more exception conditions for triggering exception processing using an exception handler, said processor being operable to select said exception handler

from among a plurality of possible exception handlers in dependence upon whether said processor is operating in said secure domain or said non-secure domain (Fig 1; Col 4, starting at line 7; Col 9, starting at line 62; Claim 1-9; exception/ interrupt handler based on whether processor/ system is operating in secure/ protected mode, or insecure/ normal modes); and programmable configurations associated therewith that control triggering of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode with any change of domain also being triggered when required (Fig 3; Col 4, line 29-67; Col 9, line 62- Col 10, line 67; Claims 1-9; controller , or mode capable processor to control exception handling based on modes/ domains)

Christie et al fails to disclose exception handlers in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table; and wherein said active exception vector table is one of a plurality of exception vector tables.

However, Knight discloses exception handlers in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table; and wherein said active exception vector table is one of a plurality of exception vector tables (Par 0007, 0015-0019; Claims 1-24; exception vector table for exception, and exceptions having corresponding operational modes such as normal, protected/ private, and IRQ modes)

Knight and Christie et al are analogous art because they are from the same field of endeavor of secure exception handling involving different operational/ execution modes. At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the teachings of Knight with Christie et al to design a method further including exception vector table in order to provide an alternative and efficient exception handling mechanism.

Regarding claim 2, Christie et al discloses apparatus wherein at least one of said exceptions is a selectable exception handled by a selectable one of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode; and at least one of said exceptions is a dedicated secure exception that is handled by a secure exception handler operating in a secure mode (Col 9, starting at line 45; Claim 2; exception handling logic).

Furthermore, Knight discloses apparatus wherein at least one of said exceptions is a selectable exception handled by a selectable one of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode; and at least one of said exceptions is a dedicated secure exception that is handled by a secure exception handler operating in a secure mode (Par 0007, 0015-0019; Claims 1-24; processor for exception handing where each exceptions has corresponding different operational modes such as normal or protected modes; and exception handling depend on mode of operations)

Regarding claim 4, Christie et al discloses apparatus having a secure exception is triggered by one of a signal on a dedicated secure exception signal input and a non secure exception signal input (Col 9, starting at line 45; Claim 1-9).

Regarding claim 5, Christie et al discloses apparatus having an exception signal input shared between secure and non-secure exceptions and a further input signal cooperating with said exception signal input to control whether a secure exception handler or a non-secure exception handler is triggered (Col 9, starting at line 45; Claim 1-9).

Furthermore, Knight discloses exception signal input shared between secure and non-secure exceptions and a further input signal cooperating with said exception signal input to control whether

a secure exception handler or a non-secure exception handler is triggered (Par 0007, 0015-0019; Claims 1-24; processor for exception handing where each exceptions has corresponding different operational modes such as normal or protected modes)

Regarding claim 6, Christie et al discloses apparatus wherein said secure exception handler is part of secure operating system operable in said secure mode (Col 9, starting at line 45;Claim 1-9).

Regarding claim 7 , Christie et al discloses apparatus wherein said non-secure exception handler is part of a non-secure operating system operable in said non-secure mode (Col 9, starting at line 45; Claim 1-9).

Regarding claims 11 and 34, Christie et al fails to disclose wherein said exception conditions includes one of more of: a secure interrupt signal exception; a mode switching software interrupt signal; a reset exception; an interrupt signal exception; a software interrupt signal; an undefined instruction exception; a prefetch abort exception; a data abort exception; and a fast interrupt signal exception.

However, Knight discloses wherein said exception conditions includes one of more of: a secure interrupt signal exception; a mode switching software interrupt signal; a reset exception; an interrupt signal exception; a software interrupt signal; an undefined instruction exception; a pre fetch abort exception; a data abort exception; and a fast interrupt signal exception (Par 0011 to 0017).

Regarding claim 13 , Christie et al discloses apparatus wherein said plurality of exception vector tables include a secure exception vector table selectable in said secure mode and a non-secure

exception vector table selectable in said non-secure mode (Col 9, starting at line 45; interrupt vectors; Col 9, starting at line 45; exception handling logic).

Regarding claims 20 and 42-43, Christie et al discloses exception trap mask register is non-writable when said processor is not in non-secure domain (Col 3, starting at line 15; Claims 5-9; debug traps).

Regarding claims 21-23, 25, 27-30, 34, 36 and 44-47, they recite the similar limitations that already addressed rejecting claims 1-10, 12-18 and 24, therefore, claims 21-23,25-33, 35-41 and 44-47 are rejected applying as above rejecting claims 1-10,12-18, 24.

13. Claims 1 and 24 are further rejected under 35 USC 103 (a) as being unpatentable over Christie et al (US 7165135 B1) in view of Dahan et al (US 7237081 B2)

Regarding claims 1 and 24, Christie et al discloses apparatus/ method for processing data, said apparatus/ method comprising:

a processor operable in a plurality of modes and a plurality of domains, said plurality of domains comprising a secure domain and a non-secure domain (Fig 1; related modes and domains; Col 4, starting at line 7, plurality of memory location associated with the plurality of the execution modes) said plurality of modes including:

at least one secure mode being a mode in said secure domain (Fig 1; secure modes and domains; Col 4, starting at line 7, plurality of memory location associated with the plurality of the execution modes) ; and

at least one non-secure mode being a mode in said non-secure domain (Fig 1; related modes and domains; Col 4, starting at line 7, normal mode and domain); wherein when said processor is

executing a program in a secure mode said program has access to secure data which is not accessible when said processor is operating in a non-secure mode (Fig 1; Col 4, starting at line 65; Col 9, starting at line 62; Claim 1)

said processor is responsive to one or more exception conditions for triggering exception processing using an exception handler, said processor being operable to select said exception handler from among a plurality of possible exception handlers in dependence upon whether said processor is operating in said secure domain or said non-secure domain (Fig 1; Col 4, starting at line 7; Col 9, starting at line 62; Claim 1-9; exception/ interrupt handler based on whether processor/ system is operating in secure/ protected mode, or insecure/ normal modes); and programmable configurations associated therewith that control triggering of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode with any change of domain also being triggered when required (Fig 3; Col 4, line 29-67; Col 9, line 62- Col 10, line 67; Claims 1-9; controller , or mode capable processor to control exception handling based on modes/ domains)

Christie et al fails to disclose exception handlers in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table; and wherein said active exception vector table is one of a plurality of exception vector tables.

However, Dahan et al discloses exception handlers in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table; and wherein said active exception vector table is one of a plurality of exception vector tables (Col 14, line 38- Col 19, line 65; specially Col 18, starts at line 46; exception/ interrupts vector table).

Dahan et al further discloses one or more exception conditions have respective programmable configurations associated therewith that control triggering of either a non-secure

exception handler operating ha a non-secure mode or a secure exception handler operating in a secure mode with any change of domain also being triggered when required (Col 16, line 1- Col 20, line 35; normal/ non-secure, and secure modes exceptions/ interrupts; SSM monitoring interrupts/ exceptions); .

Dahan et al and Christie et al are analogous art because they are from the same field of endeavor of secure exception handling involving different operational/ execution modes. At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the teachings of Dahan et al with Christie et al to design a method further including exception vector table in order to provide an alternative and efficient exception handling mechanism.

Conclusion

14. A shortened statutory period for response to this action is set to expire in 3 (Three) months and 0 (Zero) days from the mailing date of this letter. Failure to respond within the period for response will result in ABANDOMENT of the application (see 35 U.S.C 133, M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shanto M Z Abedin whose telephone number is 571-272-3551. The examiner can normally be reached on M-F from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Moazzami Nasser, can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shanto M Z Abedin

Examiner, AU 2136

/Brandon S Hoffman/

Primary Examiner, Art Unit 2136